

Construction and calibration of the DUCK (Detector of Unusual casKades) system modules

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In the High-Energy Physics field there is an active search of the origin and the nature of the Ultrahigh energy cosmic rays. These are messengers that carry information from far into the Universe, and they might also hint on direction towards new physics. This talk presents the overall hardware and software design, and the construction and calibration of DUCK (Detector system of Unusual Cosmic-ray casKades) main modules. DUCK is a new cosmic-rays detector that is being constructed at the Clayton State University campus that has resolution at the ns-level. The main scientific direction for the DUCK project is to contribute to the approach of cosmic ray event analysis using the full waveform and detector response width. Additionally, it aims to provide an independent verification of the detection of the 'unusual' cosmic ray events that were reported by the Horizon-T detector system that may be indicating direction towards the novel physics possibilities.

The European Physical Society Conference on High Energy Physics (EPS-HEP2025) 7-11 July 2025 Marseille, France

1. Introduction

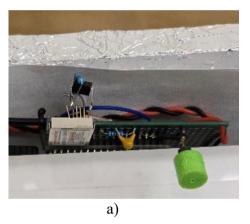
A field of physics that still has many unknowns to discover is High Energy Physics (HEP). Among the questions with unknown answers is the origin and composition of the Ultra-high Energy Cosmic Rays (UHECRs). These cosmic rays originate far from the Solar System, possibly even outside of the Milky Way galaxy. They carry information that could help us understand the universe better and provide insight into the fundamental physics principles.

The design goal of the DUCK system [1, 2, 3] is to detect and verify the existence of unusual cosmic events [4, 5]. It can eventually further innovate EAS (Extensive Atmospheric Shower) analysis methods by introducing the EAS disk width as one of the parameters. This publication aims to highlight development and construction of the detector system that is being conducted at Clayton State University campus.

2. Project Status

Out of the four modules envisioned for the DUCK system, modules #1 and #2 have been completed. While module #1 fully corresponds to the previously published specs [2,3], module #2 and all consecutive ones will have one minor change in the power supply model.

2.1 A Power Supply Saga



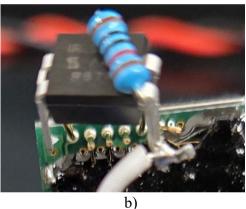


Figure 1. a) MPPC board with the power supply. b) The 'reset' circuit.

The original design of the MPPC board calls for the use of the Hamamatsu [6] power supply C11204-01 as shown in Figure 1a. It is powered by 5V, with an output from 40V to 90V. However, during the calibration of the first module and the construction of the second, numerous issues were found when using this power supply:

- COM-port communication only with outdated parity check
- Unnecessarily complicated command structure and parity calculations
- On power loss loses last setting, starts with default of 40V added Arduino controller to initialize and monitor the power supply
- With the load present, needs to be 'reset' at start-up: by accident, we discovered to short NC (not connected) pin to ground as shown in Figure 1b, not in the manual anywhere!
- No overload/short protection!

After losing 3 units (one due to accidental short-circuit, two due to reasons unknown – power supply initializes, and outputs 13V even without any load present), it was decided to use robust C9619-01 power supply instead. This supply is rated 400V-2000V, but with the right voltage

adjustment voltage from the precision potentiometer it can provide a stable -70V output. This is advantageous because the MPPC and the PMT (Photo-multiplier tube) outputs are both negative to simplify the data analysis and the ADC (analog to digital converter) settings. The updated MPPC board view is shown in Figure 2. The calibration LED is also visible in the figure. Additionally shown are the WLS fiber and its ferrule on the MPPC sensor.

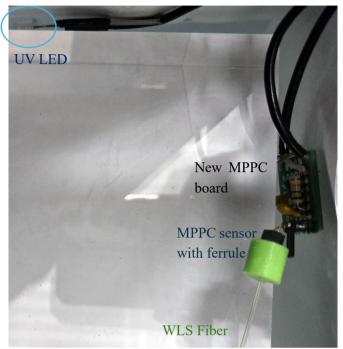


Figure 2. A new MPPC board. Also shown are the calibration UV LED, ferrule and the WLS fiber.

2.2 Current Status

With the two out of 4 modules completed, the calibration activities are taking place and the start of the construction of the remaining modules. The DAQ software is being prepared and updated to the latest C++ VS compiler. The latest update [7] was for the 2017 VS compiler. The shift to the newer one is going to take some time as the application will need to be migrated to the 64bit platform, and to ROOT v6, which requires significant source code change and a use of new rootcint that has been changed in version 6 for the ROOT into the rootcling. Some software and hardware tasks pose an opportunity to be used as student projects in the instructional labs that were recently modified and updated [8].

3. Conclusion

The current plans are to finish construction of Module 3 and 4 with the updated MPPC module, conduct calibration using MIP and LED signals, and start the separation curve study with two currently available modules.

The software future plans are to complete the ADC-DAQ control with the scripting and remote operations possibilities.

Acknowledgements

This work is supported by NSF LEAPS-MPS Award 2316097

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